PHYTEC

microMODUL-8051

Hardware-Manual

Edition April 1999

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Index of Figures and Tables

Preface

This microMODUL-8051 User's Manual describes the board's design and functions. Precise specifications for the 80C32-derivative microcontrollers can be found in the enclosed microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC microMODUL-8051

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

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The microMODUL-8051 is one of a series of PHYTEC nano/micro/miniMODULs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as insert-ready, fully functional micro- and miniMODULS which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information:

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1 Introduction

The microMODUL-8051 is a matchbox-size microcontroller board. There are two microMODUL-8051 variations available, each with ist own PCB-Numbers available. PCB-No. 1112.X accomodates a MQFP-44 package controller while PCB-No. 1103.X is suitable for a PLCC-44 package controller. They both can be populated by single-chip 80C32 microcontroller, as well as with pin-compatible derivatives (i.e. SAB-C501, SAB-C502, SAB-C504, 80C154, DS80C320 and the COM20051) These controllers generally offer special features; for instance, the COM20051 consists of an 80C32 core with an integrated ARCnet-Controller. External installation of a Hybrid-Interface enables a COM20051 based microMODUL-8051 to run at up to 255 nodes in an ARCnet network.

Precise specifications for the specific controller fitted on the microMODUL-8051 you have purchased can be found in the enclosed microcontroller manual. The microMODUL-8051 described herein is based on the standard 80C32 architecture. There follows no specific discussion of 80C32-derivative controllers, as the architecture of these derivatives is not relevant to the basic functioning of this module.

The microMODUL-8051 offers the following features:

- SBC in matchbox-size dimensions (51 x 36 mm) achieved through modern SMD technology
- improved interference safety through multi-layer technology
- controller signals and ports extend to standard-width (2.54 mm.) pins aligning board edges, allowing the board to be plugged into any target application like a “big chip”
- socketed controllers allow the flexible installation of a variety of 8051-compatible processors on the board (only PCB--No. 1103.X)
- requires a single power supply of 5V, typ. <200mA
- 128 (up to 512) kByte Flash on-board (PLCC)
- on-board Flash-programming
- no dedicated programming voltage through use of 5V-Flash-devices
- 32 (up to 128) kByte RAM on-board (SMD)
- all ports and applicable logic signals extend to pin headers at the edges of the circuit board
- flexible software-configured address decoding through a complex logic device
- bank latches for Flash and RAM integrated in address decoder
- alternate RS-232 or RS-485 interfaces
- three free chip-select signals for simple I/O-connection to external peripherals

2 Pin-Layout

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum input values are indicated in the corresponding controller manuals. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As shown in *Figure 1*, all controller signals extend to standard-width (2.54 mm) pin rows lining three sides the board (referred to as microMODUL-Connector). This allows the board to be plugged into any target application like a "big chip".

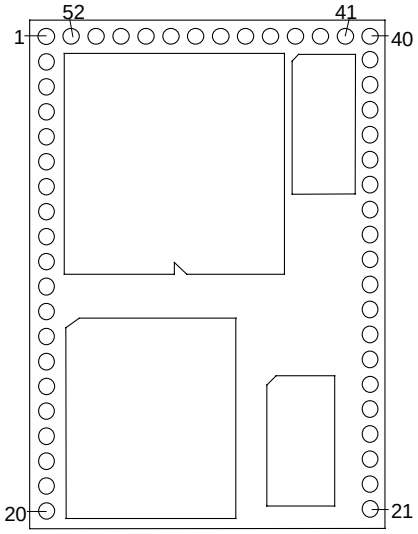


Figure 1: Pin-Layout

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the microMODUL-Connector, as well as hints about additional functions of some of the port pins. For further details please refer to the Data Sheet of the controller on the microMODUL-8051.

PIN #	Connection	Comments
1	ALE	Address latch
2...9	D0...D7	Data bus (Port 0 of the controller)
10	*Reserved 1*	Pin 34 (PLCC) / 28 (QFP) of the controllers (the function is dependent upon the controller derivative used, see below)
11	/Reset	/Reset-input port of the module
12...19	A0...A7	decoded address bus (Low-Byte)
20	GND	Ground circuit 0V
21...28	P1.0...P1.7	Port 1
29	P3.7 /RD	Port 3.7 or /RD-Signal
30	P3.6 /WR	Port 3.6 or /WR-Signal
31	P3.5 T1	Port 3.5 or Timer 1
32	P3.4 T0	Port 3.4 or Timer 0
33	P3.3 INT1	Port 3.3 or ext. INT1
34	P3.2 INT0	Port 3.2 or ext INT0
35	P3.1 TXD B	Port 3.1 or TXD (RS-232) or B (RS-485)
36	P3.0 RXD A	Port 3.0 or RXD (RS-232) or A (RS-485)
37	/CS1	predecoded Chip-Select-Signal #1
38	/CS2	predecoded Chip-Select-Signal #2
39	/CS3	predecoded Chip-Select-Signal #3
40	VCC	Supply voltage +5V=
41	VBAT	Supply voltage for battery-buffer
42	*Reserved 2*	Pin 12 (PLCC) / 6 (QFP) of the controllers (the function is dependent upon the controller derivative, see below)
43	*Reserved 3*	Pin 44 (PLCC) / 38 (QFP) of the controllers (the function is dependent upon the controller derivative, see below)
44	*Reserved 4*	Pin 1 (PLCC) / 39 (QFP) of the controllers (the function is dependent upon the controller derivative, see below)
45...52	A8...A15	Address bus (High-Byte)

Table 1: Pinout of the microMODUL-Connector

Four free or unconnected pins are available on the 80C32 (1, 12, 34, 44 (PLCC) and 6, 28, 38, 39 (QFP)). On various pin-compatible derivatives, however, these pins are utilized for special features, such as the ARCnet signals on the COM20051.

The reserved pins (denoted as *Reserved 1* through *Reserved 4*) can carry additional signals, depending on the controller derivative in use. he following table provides an overview of the pin-layout pertaining to specific controllers:

Controller	*Reserved 1*	*Reserved 2*	*Reserved 3*	*Reserved 4*
80C32	n.c.	n.c.	n.c.	n.c.
80C154	n.c.	n.c.	n.c.	n.c.
DS80C320	n.c.	n.c.	n.c.	n.c.
C501	n.c.	n.c.	n.c.	n.c.
C502	n.c.	n.c.	n.c.	n.c.
C504	COUT3	/CTRAP	VAREF	VAGND
COM20051	TXEN	/PULSE1	/PULSE2	RXIN

Table 2: Reserved Pins

n.c.= not connected

3 Jumpers

For configuration purposes, the microMODUL-8051 has 4 soldering jumpers, some of which have been configured prior to delivery. *Figure 2* illustrates the numbering of the Jumper-pads, while *Figure 3* indicates the location of the Jumpers on the board. . All soldering jumpers on the microMODUL-8051 are located on its top side.

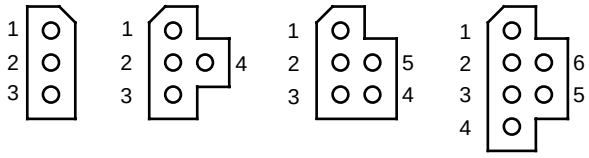
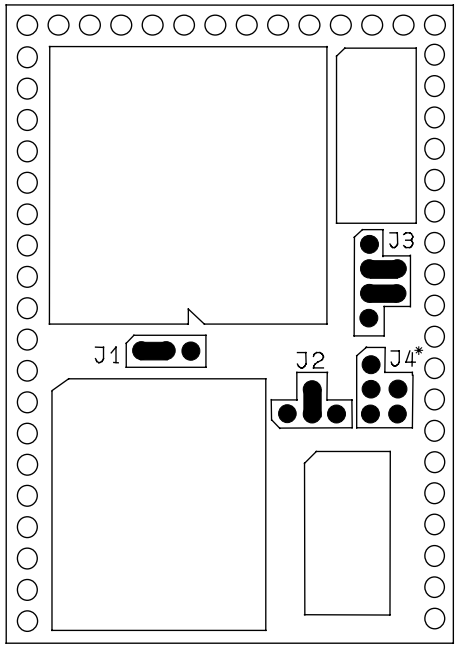


Figure 2: Numbering of the Jumper-pads



✳ Configuration dependent on the controller mounted on the microMODUL-8051

Figure 3: Location of the Jumpers (view of the component side)

The Jumpers (J = solderable jumper) have the following functions:

	Default-Setting	**Alternate-Setting**
J1	(1+2) external ROM/ Flash active	(2+3) internal ROM/Flash active
J2, J3	(2+4) (2+6) (3+5) pins 35 and 36 carry RS-232 signals from the on-board transceiver	pins 35 and 36 carry TTL signals from the controller's serial port or RS-485 signals *(refer to section 3.2)*
J4	Configuration of special features of the particular controller fitted on the module*(refer to section 3.1)*	

Table 3: Jumper Settings

3.1 Special Features J1, J4

Jumpers J1 and J4 are used to activate the special features of the particular controller fitted on the module.

- **Execution out of internal or external program memory**
  At the time of delivery, Jumper J1 is preconnected between pads 1+2. This default configuration means that the program stored in the external program memory is executed after a Reset. In order to allow the execution of a specific controller's internal program memory, the pads 2+3 on Jumper J1 must be connected.

  The following configurations are possible:

Code-Fetch	J1
execution from external program memory	1+2
execution from internal program memory	2+3

- **Additional Controller Peripherals**

  Jumper J4 configures previously unused pins (1, 12, 34, 44 (PLCC) and 6, 28, 38, 39 (QFP)) on special derivatives of the 80C32. On several of these derivative controllers, these pins are utilized to connect to a supplemental power source. Other derivatives use the pins for connection to special peripheral devices integrated on-chip. The following table provides an overview of the configuration of Jumper J4 for specific controllers.

  Please note that this table is not a comprehensive list of all possible configurations, as it does not include all 80C32 compatible controllers that can be mounted on the board.

  For others than the listed controllers, the circuit diagram of the microMODUL-8051 and the pinout of such controllers will specify the settings of the respective Jumpers which enable external peripheral connectivity. This could necessitate that required - but unassigned - signals have to be conducted externally via the reserved module pins (10, 42...44).

Controller	J4	Comments
80C32	3+4	Pin 44 (PLCC) / 38 (QFP) on VCC
80C154	3+4 1+2	Pin 44 (PLCC) / 38 (QFP) on VCC Pin 17 (QFP) on GND
DS80C320	1+2 3+4	Pin 23 (PLCC) / 17 (QFP) on GND Pin 44 (PLCC) / 38 (QFP) on VCC
C501	3+4	Pin 44 (PLCC) / 38 (QFP) on VCC
C502	3+4	Pin 44 (PLCC) / 38 (QFP) on VCC
C504	2+3 4+5	Pin 23 (PLCC) / 17 (QFP) on VCC Pin 44 (PLCC) / 38 (QFP) on module connection 43
COM20051	2+5 3+4	Pin 23 (PLCC) / 17 (QFP) on module connection 43 Pin 44 (PLCC) / 38 (QFP) on VCC

3.2 Serial Interface J2, J3

With Jumpers J2 and J3 different signal levels and signal qualities can be applied to the serial interface pins of the microMODUL-8051 (Pins 35 and 36). These pins carry either the TTL-signals of the controller's serial interface, the signals of the on-board RS-232 transceiver or the signals of the on-board RS-485 transceiver. At the time of delivery the RS-232 interface is active by default.

The following signal levels and qualities can be configured:

Signal Quality	J2	J3
RS-232	2+4	2+6 3+5
RS-485	2+3	1+2 3+4
TTL	1+2	2+3

4 Memory-model

The microMODUL-8051 allows flexible address decoding which can be adjusted by software to different memory-models. A Hardware-RESET activates a default memory configuration that is suitable for a variety of applications. However, this memory-model can be changed or adjusted at the beginning of a particular application.

Configuration of the memory is done within the address decoder by means of decoder internal registers: two control registers, one address register and one mask register. All named registers are carried out as Write-Only-Registers with access to the XDATA-memory of the controller. There are two distinct address areas - selectable by means of the bit IO-SW in control register 1 - by which the registers can be accessed (refer to the description of the bit IO-SW below). Due to a lack of read-access, a copy of all register contents should be maintained within the application. Reserved bits may not be changed during the writing of the register; contents must remain at 0. A Hardware-RESET erases all registers, while preserving the configuration of the default memory.

In the event that you use the FlashTools – PHYTEC'S proprietary firmware allowing convenient on-board Flash-programming - it should be noted that the address FA16 will be preset at the start of your application software (refer to the section *4.1* 'Control Register 1'). This is to be noted upon installation of the software copy of the register contents.

The following figure displays the default memory-model:

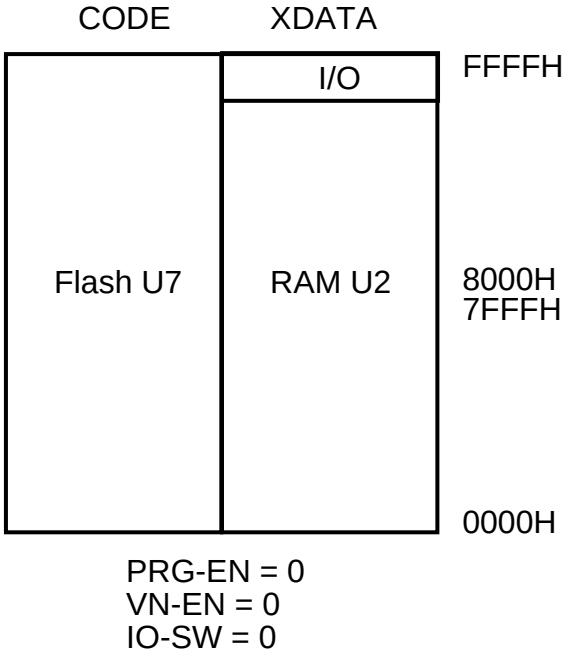


Figure 4: Default-memory-model after Hardware-Reset

It should be noted that in case of modules equipped with only 32 kByte RAM, the RAM-memory block U2 in the XDATA-area is mirrored to the XDATA-area starting at 8000H. In this case U2 is located in the XDATA-address range from 0000H - 7FFFH, as well as from 8000H - FFFFH. The corresponding current I/O-area is concentrated in an XDATA-address area in which there is no access to any existing RAM.

In the following sections the registers of the address decoder for configuration of the memory are explained:

4.1 Control Register 1

Control Register 1 (Address 7C00H / FC00H)							
Bit 7							Bit 0
PRG-EN	IO-SW	*Res.*[1]	VN-EN	FA18	FA17	FA16[2]	FA15

Bit invalid in programming-model (refer to PRG-EN)
Bit valid only in programming-model (refer to PRG-EN)

PRG-EN: Activates the special Flash-programming memory model (PRG-EN = 1). This configuration is used within FlashTools[3] for Flash-programming. On account of existing restrictions it is either of no or of restricted use in the user's application.
In this model, 32 kByte Flash memory located within the address range 0000H - 7FFFH is accessible, as well as 32 kByte RAM within the range 8000H - FFFFH. The Flash memory can only be written in the XDATA-area and can only be read from the CODE-area. The RAM can be read from and written to in the XDATA-area. RAM can also be read from the CODE-area. The address line A15 of the Flash is derived from the Control Register 1 (Bit 0, FA15) only in the programming configuration. In the Runtime execution-configuration (PRG-EN = 0), the address line A15 of the controller is attached directly to the Flash device.
The bit IO-SW is also relevant to the programming configuration; whereas the bit VN-EN is not relevant.

1: Reserved bits may not be changed during the writing of the register; contents must remain 0
2: In the event that you use the FlashTools - a firmware allowing convenient on-board Flash-programming - it should be noted that the address FA16 will be preset at the start of your application software. This is to be noted upon installation of the software copy of the register contents.
3: PHYTEC firmware allowing convenient on-board Flash-programming. Upon delivery of the module, this firmware is already resident in the Flash device.

The following figure illustrates the programming configuration (the I/O-field is not represented):

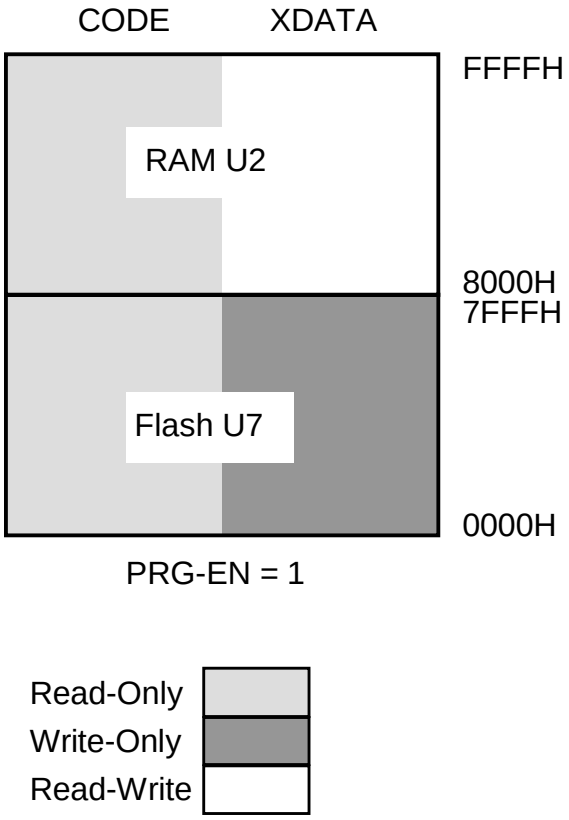


Figure 5: Memory-model for Flash-Programming

IO-SW: By means of this bit the I/O-area of the module can be mapped either to the upper or to the lower 32 kByte of the address space. After a Hardware-Reset (IO-SW = 0), the I/O-area is located in the address area from FC00H to FFFFH. Following setting of the IO-SW-bit, the I/O-area is located in the address area from 7C00H to 7FFFH.
This I/O-area generally consists of 4 blocks of 256 bytes. In three of these blocks the address decoder provides a precoded Chip-Select-Signal which simplifies the connection of peripheral hardware to the module.

These Chip-Select-Signals are activated by XDATA-access (Read-Write access) to the corresponding address area. The fourth block is reserved for accessing the register internal to the decoder (Write-Only access). Hence, this block is not available for connection of peripheral hardware to the module.

The following diagram illustrates the partitioning of the I/O-area:

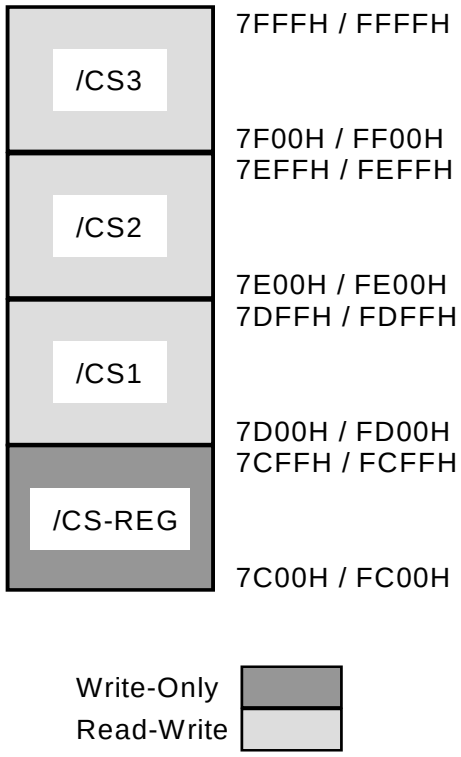


Figure 6: Partitioning of the I/O-Area

Given this partition, /CS1 through /CS3 function as the available free Chip-Select signals. The signal /CS-REG is solely a signal internal to the decoder, which is necessary in order to access the internal register. This latter signal is not available. Connection of peripheral devices to the area of /CS-REG should not take place under any circumstances in order to maintain the correct function of the FlashTools[1] for programming of the Flash. The internal register is to occupy only the address ranges 7C00H - 7C03H and/or FC00H - FC03H. The rest of the /CS-REG block remains unused and is reserved for future expansion.

VN-EN: This bit enables free selection of von-Neumann memory[2] within the address space of the controller. A Reset renders a Harvard[3]-Architecture available as the default configuration. Von-Neumann memory is especially useful when programming code is to be downloaded and subsequently run during Runtime, as is the case with a Monitor program. The location of the optional von-Neumann memory is defined through the address- and mask registers (see below).
Following a Hardware-Reset (VN-EN = 0) the settings in the address- and mask registers are not released, which means that no von Neumann-memory is available. After setting the bit (VN-EN = 1), the settings in the address- and mask registers are valid and incorporated in access addressing. This bit is only relevant in the Runtime-model (PRG-EN = 0). In the Programming-model (PRG=1) it is unimportant and ignored.

1: PHYTEC firmware allowing convenient on-board Flash-programming. Upon delivery of the module, this firmware is already resident in the Flash device.

2: Memory area in which no difference is made between CODE- and XDATA-access. This means that both accesses use the same physical memory device, usually a RAM.

3: Memory area in which CODE and XDATA-accesses use physical different memory devices. CODE-access typically uses a ROM or Flash device, whereas XDATA-access uses a RAM.

FA[18..15]: The module can be equipped with an optional 512 kByte Flash memory. As the controller's address space is limited to 64 kByte, the remainder of the Flash memory can only be accessed by means of bank memory switching.

In the Runtime-model (PRG-EN = 0), 64 kByte banks can be switched by controlling the high address lines A[18..16] for the Flash through software. For this purpose, register bits FA[18..16] of the address decoder provide a latch to which the desired higher addresses can be written.

Of particular note is the bit FA15, which is solely relevant in the programming-model (PRG-EN = 1). As only 32 kByte of Flash can be accessed in this model, it serves as address line A15 for the Flash memory. In the Runtime-model (PRG-EN = 0) with a 64 kByte Flash memory area, to contrast, the addres line A15 of the controller is attached directly to the Flash.

Bits FA[18..16] are dependent on the hardware configuration of the module and function as described above only if Flash devices of at least 512 kByte are used on the board.

4.2 Control Register 2

Control Register 2 (Address 7C01H / FC01H)							
Bit 7							Bit 0
N/A[1]	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	RA16	*Res.*[2]

RA16: The module can accommodate a 128 kByte RAM. As the controller's address space is limited to 64 kByte, the remainder of the RAM can only be accessed by means of bank switching.
64 kByte banks can be switched by setting the high address-line A16 through software. For this purpose, register bit RA 16 of the address decoder provides a Latch to which the desired higher addresses can be written.
The function of this bit is dependent on the hardware configuration of the module and functions as described above only in connection with RAM devices of at least 128 kByte.

[1]: N/A: Not Accessible
[2]: Reserved bits are not to be changed, the default value (0) has to remain.

4.3 Address Register

The address register 7C02H / FC02H functions in conjunction with the mask register (see below) to define the von-Neumann[1]- and Harvard[2]-memory in the controller's addressing area. By setting the bit VN-EN in control register 1, the values of the address and the mask register become valid for the definition of the von-Neumann and the Harvard addressing space and are used for address decoding (refer to section *4.1* 'Control Register 1'). The location of one or more Harvard areas can be configured with both registers.
The remaining sections of the addressing area are configured as von-Neumann area in which RAM is accessible through XDATA as well as through CODE.

The mechanism through which the areas are differentiated is based on a comparison of the current address with a predefined address pattern of variable width. If the relevant bit positions of the addresses conform to one another, access occurs according to the Harvard-architecture. In the case of nonconformity, access occurs according to the von-Neumann-architecture.

Address Register (Address 7C02H / FC02H)							
Bit 7							Bit 0
HA15	HA14	HA13	HA12	HA11	HA10	*Res.*[3]	*Res.*

The address register holds the address pattern mentioned above. Each bit of the pattern is compared with the corresponding address line of the controller (HA15 with A15, ..., HA10 with A10). As address lines A15 .. A10 are used to define Harvard addressing space, only Harvard-fields of at least 1 kByte can be configured. Areas smaller than 1 kByte can not be configured.

1: Memory area in which no difference exists between CODE- and XDATA-access. This means that both accesses use the same physical memory device, usually a RAM.

2: Memory area in which CODE and XDATA-accesses use different physical memory devices. Usually CODE-access uses a ROM or Flash device, whereas XDATA-access uses a RAM.

3: Reserved bits are not to be changed, the default value (0) must remain.

4.4 Mask Register

The mask register (addresses 7C03H / FC03H) serves the masking of single bits in the address register (see above). Following a Hardware-RESET, all bits within the address register are relevant. By setting the individual bits in the mask register, all corresponding bits in the address register will no longer be subject to an address comparison.

Mask Register (Address 7C03H / FC03H)							
Bit 7							Bit 0
MA15	MA14	MA13	MA12	MA11	MA10	*Res.*[1]	*Res.*

Please note that in the case of a board populated with a single 32 kByte RAM, the memory area is mirrored within the controller's addressing area. On account of the insufficient utilization of A15 in this configuration, memory accesses to addresses higher than 8000H are reduced to accesses to the memory area from 0000H to 7FFFH. This should be taken into consideration when choosing the memory-model. Otherwise, function failure could result from overlapping access.

[1]: Reserved bits are not to be changed, the default value (0) has to remain.

The following examples of different combinations of the address- and mask registers illustrate these functions (X = specific bit irrelevant):

Address-Reg.	Mask-Reg.	Comments (only for VN-EN = 1)
1XXXXX00b	01111100b	Harvard 8000H-FFFFH, Von-Neumann 0000H-7FFFH
0XXXXX00b	01111100b	Harvard 0000H-7FFFH, Von-Neumann 8000H-FFFFH
11111100b	00000000b	Harvard FC00H-FFFFH, Von-Neumann 0000H-FBFFH
010X0000b	00010000b	Harvard 4000H-43FFH and 5000H-53FFH, Von-Neumann 0000H-3FFFH, 4400H-4FFFH and 5400H-FFFFH
10000000b	00000000b	Harvard 8000H-83FFH, Von-Neumann 0000H-7FFFH and 8400H-FFFFH
10100X00b	00000100b	Harvard A000H-A7FFH, Von-Neumann 0000H-9FFFH and A800H-FFFFH

Reserved bits without function for address decoding (refer to description of the register)

X = irrelevant (on account of a bit set in the mask register)

The last example in the table is further illustrated by the following figure:

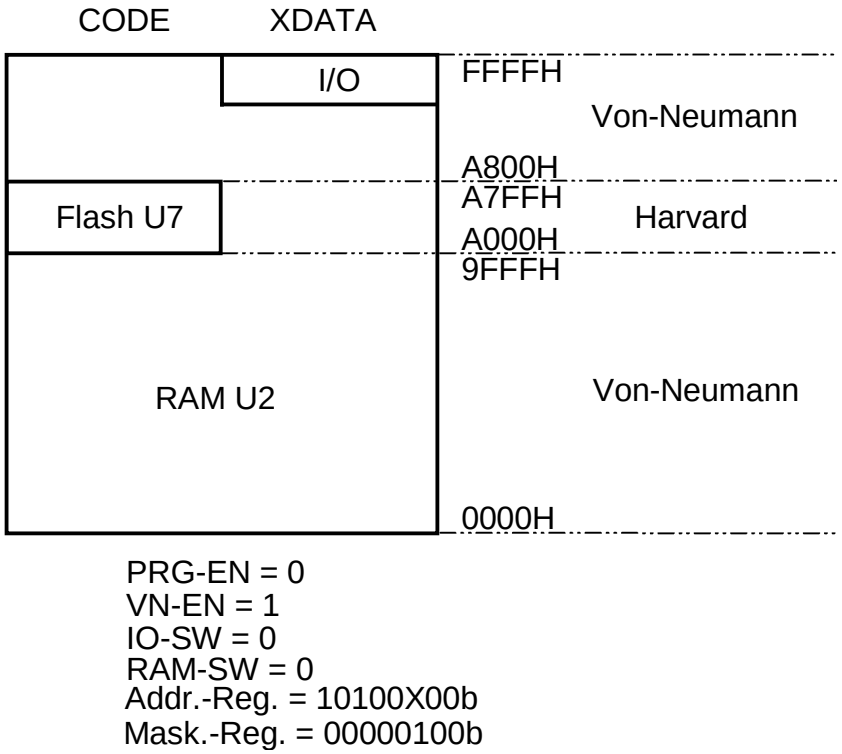


Figure 7: Example of a Memory-model

5 Flash-Memory

Flash is a highly functional means of storing non-volatile data. Having the microMODUL-8051 equipped with a Flash device makes this modern technique available. The microMODUL-8051 can house a Flash device of type 29F010 with two banks of 64 kByte each or of type 29F040 with 8 banks of 64kByte each.

Use of Flash devices allows incorporation of on-board programming capability. The Flash devices are programmable with 5V=. Consequently, no dedicated programming voltage is required. A firmware to programm the Flash device (the so-called FlashTools) is pre-installed in the first bank (bank 0) of the Flash device. Hence the total memory available is 64 kByte or 448 kByte (*refer to Figure 8*).

Should this software be erased from the Flash device without having a back-up or an equivalent replacement, reprogramming is no longer possible!

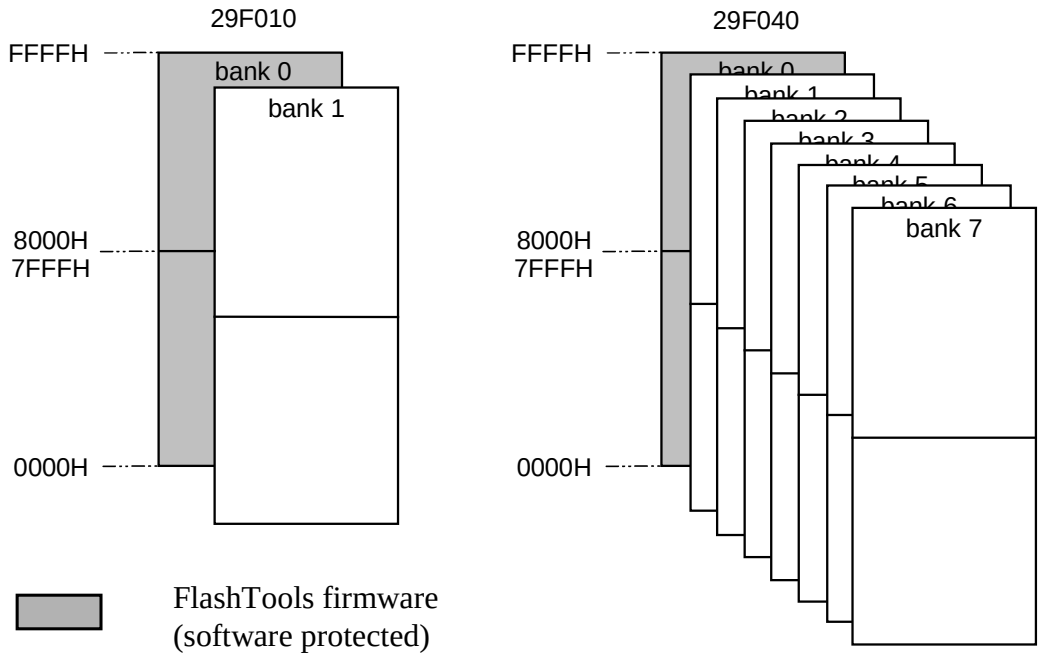


Figure 8: Memory Areas of the Flash Device

Please note that this firmware protects itself against any intentional or accidental erasure or copy-over. As the Flash device’s hardware protection mechanism is not utilized, protection is limited to the software level. In the event that you might wish to download your own programming algorithms or tools into the Flash, please ensure that a programming tool remains in the Flash memory. Refer to the “QuickStart Instructions" for a detailed description of the on-board programming.

Use of a Flash device as the only code memory results in no or only a limited usability of the Flash memory as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash-internal programming process, the reading of data from Flash is not possible. Hence, for Flash programming, program execution must be transferred out of Flash (such as into von-Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 Erase-/Program-cycles.

6 Battery Buffer

The battery that buffers the memory is not otherwise essential to the functioning of the microMODUL-8051. However, this battery buffer embodies an economical and practical means of storing nonvolatile data.

The VBAT-input at pin 41 is intended to connect to an external battery. As of the pressing of this manual, a lithium battery is recommended for use with the module as it offers relatively high capacity at low discharge. In the event of a power failure at Vcc, RAM memory will be buffered by connected battery via VBAT.

Power consumption depends on the components used and memory size. This is typically < 1 µA (max. 100 µA) per RAM device installed on the microMODUL-8051.

For reasons of operating safety, please be advised that despite battery buffer, changes in the data content within the RAM can occur given disturbances. The battery buffer does not completely remove the danger of data destruction.

7 Technical Specifications

The physical dimensions of the microMODUL-8051 are represented in *Figure 9*. The module's profile is about 10 mm thick, with a max. height of the components of 3.5 mm on the back-side of the board and approx. 5 mm on the top-side. The board itself is approx. 1.5 mm thick.

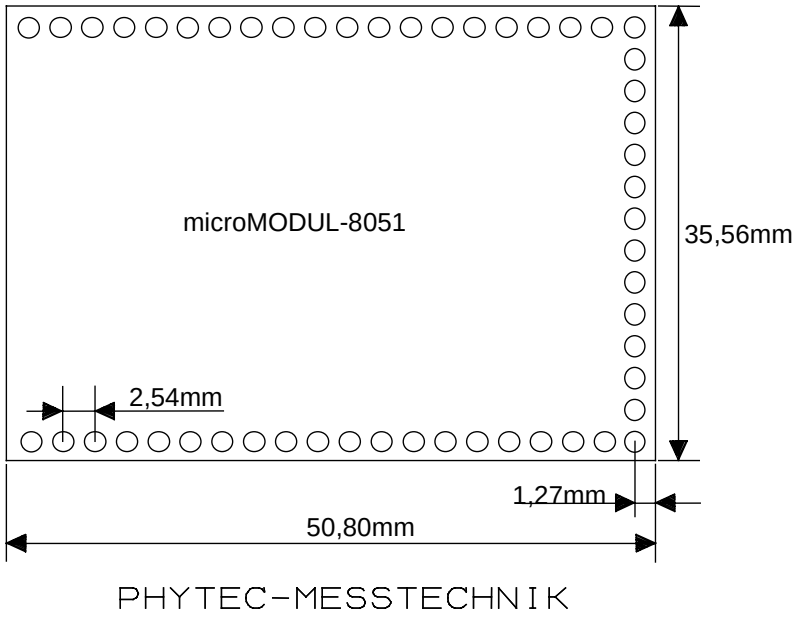


Figure 9: Physical Dimensions

Additional specifications:

- Dimensions: 50.8 x 35.56 mm., ±0,01mm
- Weight: approximately 20 g with 128 kByte RAM device, socketed Flash device controller
- Storage temperature: -40°C to +90°C
- Operating temperature: standard 0°C to +70°C, extended -40°C to +85°C
- Humidity: maximum 95% r.F. not condensed
- Operating voltage: 5 V. ±5%, VBAT 3V ±20%
- Power consumption: maximum 290 mA, typ. 175 mA at 40 MHz oscillator frequency and 32 kByte RAM
- Power consumption with battery buffer: 10 µA per RAM-device, typically 1 µA per RAM-device at +20°C

This specifications describe the standard configuration of the microMODUL-8051 as of the pressing of this manual.

Please note that utilizing the battery buffer for the RAMs the storage temperature is only 0°C to +70°C.

8 Hints for Handling the Module

When changing controllers please ensure that appropriate PLCC tools are used and that the socket and all components remain free from intrusive damage. Any controller used on the module must be pin-compatible with the 80C32, and all special hardware features must be compatible with the layout of the board. Special consideration should be given to the unused 80C32 pins. It is absolutely necessary to check the position of Jumper J4, as an improper setting cause irreparable damage to the controller.

Removal of the standard quartz or oscillator is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while unsoldering the clock. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Index

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How would you improve this manual?

Did you find any mistakes in this manual? page

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